REMARKS

Prior to this Reply, Claims 1-18 and 20-101 were pending. Through this Reply, Claims 23 and 24 have been amended. No claims have been cancelled or added. Accordingly, Claims 1-18 and 20-101 are now at issue in the present case.

I. Allowable Subject Matter

Applicant notes, with thanks, the Examiner's allowance of Claims 30-49 and 64-101. Such claims have not been amended. Accordingly, Applicant submits that Claims 30-49 and 64-101 are still allowable.

II. Rejection of Claims 1, 6, 9, 11 and 12 Under 35 U.S.C. § 103(a)

The Examiner rejected Claims 1, 6, 9, 11 and 12 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,445,530 to Baker (hereinafter "Baker") in view of U.S. Patent No. 5,859,518 to Vitunic (hereinafter "Vitunic"). Applicant respectfully traverses the Examiner's rejection because the references fail to disclose each and every limitation of the rejected claims.

With respect to Claim 1, the references alone or combination do not disclose a driver having a current control device for a voice coil motor in a disk drive, comprising: "a sensor to sense a coil current in said voice coil motor; a transconductance amplifier to detect an error current by comparing said coil current and a command current; and a compensator to integrate said error current into said coil current," as required by Claim 1.

The Examiner states that Baker discloses the claimed limitations of a sensor (Baker, Fig. 10: element 168) to sense a coil current in a voice coil motor and a transconductance amplifier

(Baker, Fig. 12, element 216) to detect an error current by comparing said coil current and a command current (Baker, Col. 8, lines 40-45). Applicant respectfully disagrees because, in Baker, the coil current is not compared to a command current to detect an error current, as required by Claim 1.

Baker provides an apparatus for supplying bi-directional load current to a load 126. Four current sensing metal oxide semiconductor field effect transistors (FET) 200 are configured to form an H-bridge with the load 126. Each transistor 200 has separately insulated gate 192, source 186, drain 190 and sense terminal 202. A source to drain conductivity is determined in relation to a voltage applied to the gate terminal, and a sense current I_{SENSE} from the sense terminal 202 is determined in relation to a magnitude of source to drain current. Drive voltages are applied by driver circuits 206 to the gate terminals 192 of alternating pairs of the transistors 200 to apply the load current I_L 226 to the load 126. The sense current I_{SENSE} is used by a clamp circuit 208 used to provide adaptive, closed-loop clamping of the drive voltages at levels sufficient to maintain the non-load current conducting transistors 200 in a quiescent state (Baker, Abstract, Figs. 10 and 12).

Each clamp circuit 208 clamps the lowest voltage levels output by the driver circuit 206 to levels sufficient to maintain a FET 200 in a quiescent state when not used to conduct load current (Col. 7, lines 44-48). In Fig. 12, the clamp circuit 208 uses a sense current I_{SENSE} output from the sense connection 202 of the FET 200 as a feedback signal to apply an appropriate gate voltage V_{GS} to the gate 192 to maintain the drain current I_D at a quiescent level. The circuit of Fig. 12 utilizes a transconductance amplifier 216 to provide an output voltage in relation to the difference between the I_{SENSE} current from the sense connection 202 and a reference current I_{REF} from a reference current source 218. At times when the driver circuit 206 is not passing load

current through the FET 200, the transconductance amplifier 216 will operate to increase or decrease the drain current I_D to maintain an appropriate quiescent state for the FET 200, and will not otherwise interfere with the operation of the FET 200 to pass load current to the coil 126. (Baker, Col. 8, lines 39-51).

Accordingly, in Baker, the coil current I_L is not compared to a command current to detect an error current. This is because the coil current I_L flowing through the coil 126 and the sense current I_{SENSE}, from the sense connection 202, are not the same. It is I_{SENSE} current that is input to the transconductance amplifier 216, not the coil current I_L. The sense current I_{SENSE} input of the transconductance amplifier 216 is not a coil current as claimed.

Further, the reference current I_{REF} input to the transconductance amplifier 216 is not a command current as claimed because the current I_{REF} is not the current that is not intended (i.e., commanded) to flow through the coil 126. Accordingly, the transconductance amplifier 216 does not "detect an error current by comparing said coil current and a command current," as required by Claim 1.

Yet further, the output of the transconductance amplifier 216 is not an error current that can then be integrated into the coil current by a compensator, as required by Claim 1. Rather, the output of the transconductance amplifier 216 "will operate to increase or decrease the drain current I_D to maintain an appropriate quiescent state for the FET 200, and will not otherwise interfere with the operation of the FET 200 to pass load current to the coil 126" (Baker, Col. 8, lines 45-51). If Claim 1 is once again rejected, Applicant respectfully requests that the Examiner specifically point to language and elements in Baker that disclose the aforementioned claim limitations.

Further, as the Examiner admits, Baker does not disclose: "a compensator to integrate said error current into said coil current," as required by Claim 1. However, the Examiner contends that Vitunic teaches a current control device having a sensor to sense a coil current in a motor (Fig. 7: ISNSA); a transconductance amplifier (Fig. 7: element 234) to detect an error current by comparing an actual speed to a desired speed (Col. 15, lines 42-44); and a compensator to integrate the error current into a coil current (Col. 15, lines 44-53). Applicant respectfully disagrees.

The symbol ISNSA in Fig. 7 of Vitunic represents current in a winding (Vitunic, Col. 15, lines 51-53), and is not a sensor for sensing a coil current as claimed. Further, the transconductance amplifier 234 does not detect an error current by comparing a sensed coil current and a command current, as required by Claim 1. Rather, the transconductance amplifier 234 receives a first voltage signal that is representative of the actual motor speed and another voltage signal that is representative of a desired motor speed (Vitunic, Col. 15, lines 2-8).

In addition, the output of the transconductance amplifier 234 develops a voltage across the capacitor 250, which is a mathematical integration of the error current over time. The voltage signal across the capacitor 250 is representative of a level of motor current required in the windings for eliminating the speed error. The voltage signal across the capacitor 250 is compared to the signal ISNS by the transconductance amplifier 236 (Vitunic, Col. 15, lines 44-51).

Accordingly, the capacitor 250 does not "integrate [an] error current into [a] coil current," as set forth in Claim 1. Indeed, the voltage across the capacitor 250 is compared to the signal ISNS by the transconductance amplifier 236, which generates an output representative of a

change to the winding current required for maintaining the desired motor speed (Vitunic, Col. 15, lines 54-57). As such, Vitunic does not disclose each of the limitations required by Claim 1.

Further, there is no motivation in the references themselves for combining Baker and Vitunic. Applicant believes that, if the references were combined, the combination would result in a non-functioning system, rather than provide a benefit such as reducing speed error as suggested by the Examiner. Applicant believes that Baker's driver does not need a compensator and Applicant is at a loss as to how Baker would use a compensator. In Baker, a clamp circuit, connected to the gate terminals of a FET transistor, uses the sense current from the associated sense terminal of the FET transistor in a closed-loop fashion to adaptively maintain the FET transistor in a quiescent state when the drive voltage drops to a value that would otherwise make the FET transistor enter a nonconductive state (Baker, Col. 3, lines 19-25).

Specifically, in Fig. 12 of Baker, the clamp circuit 208 uses a sense current I_{SENSE} output (not a coil current I_L) from a sense connection 202 of the FET 200 as a feedback signal to apply an appropriate gate voltage V_{GS} to the gate 192 of the FET 200 for maintaining the drain current I_D at a quiescent level. The transconductance amplifier 216 provides an output voltage in relation to the difference between the I_{SENSE} current from the sense connection 202 and the reference current I_{REF}. In this way, the direction and magnitude of the coil current can be readily varied to provide robust response, even at very low, fast changing coil currents (Baker, Col. 3, lines 25-28).

In contrast, in Fig. 7 of Vitunic, the output of the transconductance amplifier 234 develops a voltage across the capacitor 250, which is a mathematical integration of the error current over time, representative of a level of motor current required in the windings for eliminating the speed error. Applicant believes that the capacitor 250 cannot be integrated into

the circuit of Baker because the capacitor 250 develops said voltage over time and would interfere with Baker's goal of readily varying the direction and magnitude of the coil current to provide robust response, even at very low, fast changing coil currents. Baker appears to teach away from integrating over time to develop correction. Instead, Baker requires immediate and robust response to fast changing coil currents.

Yet further, nowhere in Baker is speed control even mentioned. Baker is not concerned with speed control or eliminating speed error. Rather, Baker is concerned with using a sense current in a closed-loop fashion to adaptively maintain a transistor in a quiescent state when the drive voltage drops to a value that would otherwise make the transistor enter a nonconductive state. These two goals have nothing to do with one another.

Furthermore, the Examiner has not explained how the capacitor 250 in Fig. 7 of Vitunic can be integrated into the circuit in Fig. 12 of Baker. The Examiner has also not explained how the voltage across the capacitor 250, representing a level of motor current required in the windings for eliminating the speed error, can in any way be used in the circuit 12 of Baker as a feedback signal to apply an appropriate gate voltage V_{GS} to the gate 192 of the FET 200 for maintaining the drain current I_D at a quiescent level. Indeed, as mentioned above, Applicant believes that including the capacitor 250 into Baker's system would disable Baker's system. As such, one of ordinary skill in the art would not look to Vitunic to modify Baker to achieve the invention as claimed in Claim 1.

For at least the above reasons, Applicant submits that Claim 1 is patentably distinguishable from Baker and Vitunic, both alone or in combination. For at least the same reasons, Applicant submits that all claims depending from Claim 1 (i.e., Claims 2-13) are likewise patentably distinguishable from Baker and Vitunic (both alone and in combination).

With respect to Claim 10, Baker does not disclose that "said command current is received at said driver from a microcontroller," as required by such claim. There is no command current in Baker that is then compared to a sensed coil current by a transconductance amplifier. The DSP 144 and driver 148 in Fig. 2 of Baker appear to be mentioned by the Examiner totally out of context. The Examiner has not shown that Baker discloses receiving a command current from the DSP 144 of Fig. 2 that is compared to a sense current by a transconductance amplifier to detect an error. For at least the above reasons, Applicant believes that Claim 10 is patentably distinguishable from Baker and Vitunic, both alone and in combination.

With respect to Claim 11, Vitunic does not disclose "said compensator coupled to said transconductance amplifier, said compensator including a capacitor," as required by such claim. As discussed above in relation to Claim 1, in contrast to the claimed transconductance amplifier, Vitunic's transconductance amplifier 234 does not compare a commanded current to a sensed coil current as claimed. Vitunic specifically states that: "The OCV 242 receives the signal COMMCLK and provides a signal to an inverting input of the transconductance amplifier 234 that is representative of the actual motor speed. A non-inverting input of the transconductance amplifier 234 is coupled to receive a voltage signal that is representative of a desired motor speed from a terminal VSPEED of the controller 200." (Vitunic, Col. 15, lines 2-8). Further, as noted above in relation to Claim 1, Vitunic's capacitor 250 is not a compensator. Also, the voltage across the capacitor 250 represents a motor current to correct a speed error, which clearly indicates that the capacitor 250 is not a compensator capacitor to integrate an error current into said coil current, wherein the error current is detected by comparing a sensed coil current to a command current. Therefore, for at least the additional reasons, Applicant submits that Claim 11 is patentably distinguishable from Baker and Vitunic, both alone and in combination.

With respect to Claim 12, such claim requires that "the transconductance amplifier includes a first input and a second input, such that said coil current is coupled to the first input of the transconductance amplifier, and said command current is coupled to the second input of the transconductance amplifier, wherein the transconductance amplifier detects said error current by determining the difference between the coil current and the command current." The Examiner states that the limitations of Claim 12 are met by the combination of Baker and Vitunic, and directs Applicant's attention to the capacitor 252 in Fig. 7 of Vitunic. However, the Examiner has not explained how the capacitor 252 is in any way related to the above-quoted limitations. Therefore, for at least this additional reason, Applicant submits that Claim 12 is patentably distinguishable from Baker and Vitunic.

III. Rejection of Claim 4 Under 35 U.S.C. § 103(a)

The Examiner rejected Claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Baker and Vitunic as applied to Claim 1 above, and further in view of U.S. Patent No. 5,731,935 to Lian et al. (hereinafter "Lian"). Applicant respectfully traverses the Examiner's rejection.

In rejecting Claim 4, the Examiner simply suggests that adding a second coil to Baker and Vitunic would be obvious, and provides velocity control. However, the Examiner has not shown how a second coil would be added to Baker and Vitunic to result in a working system in either case. Both Baker and Vitunic are designed for single coil loads, and Applicant believes adding an additional coil would require substantial redesign and rework of their systems by one of ordinary skill in the art. Neither reference even mentions adding a second coil. Further, Lian is directed to a voice coil for a tape drive not a voice coil for a disk drive. As such, Applicant submits the coils 40 in Lian are not suitable for the drivers in Baker and Vitunic. For at least

these additional reasons, Applicant submits that Claim 4 is patentably distinguishable from Baker, Vitunic and Lian (alone and in combination).

IV. Rejection of Claims 2, 3, 6, 7, 8, 11 and 13 Under 35 U.S.C. § 103(a)

The Examiner rejected Claims 2, 3, 6, 7, 8, 11 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Baker and Vitunic as applied to Claim 1 above, and further in view of U.S. Patent No. 5,838,515 to Mortazavi et al. (hereinafter "Mortazavi"). Applicant respectfully traverses the Examiner's rejection.

Applicant notes that Claims 2, 3, 6, 7, 8, 11 and 13 depend directly or indirectly from Claim 1. Accordingly, such claims are believed to be allowable for the reasons provided above with respect to Claim 1. Nevertheless, some of such claims may also be allowable for additional reasons and some of those reasons are provided below.

With respect to Claim 2, the references alone or in combination do not disclose "a force couple created by said current in said voice coil motor," as required by Claim 2. The Examiner cites Col. 10, lines 20-26 of Mortazavi in stating that Mortazavi teaches a force couple created by the current in the VCM. Applicant believes that Mortazavi does not even mention the phrase "force couple." Col. 10, lines 20-25 of Mortazavi simply states: "A resultant current flows through the coil 24, either in the forward or reverse direction, causing a reaction force to be applied to the head positioner 18 during seek deceleration in order to stop the head relative to the disk at a desired track location in the shortest practical time with minimum heat being generated within the motor chip 26." However, this has nothing to do with a force couple created by a current in a voice coil motor, as claimed in Claim 2.

Generally, a force couple is defined by two parallel forces of equal magnitude, but opposite direction, applied to a structure at equal distances from the center of the mass. Mortazavi does not describe, show or even mention such a function. For at least this additional reason, Applicant believes that Claim 2 is patentably distinguishable from Baker, Vitunic and Mortazavi (alone and in combination).

With respect to Claim 3, the references alone or in combination do not disclose "a current sense amplifier coupled to said transconductance amplifier to amplify a voltage across said sensor," as required by Claim 3. The driver amplifier 64 in Fig. 2 of Mortazavi (which is relied on by the Examiner in rejecting Claim 3) is a coil driver amplifier, not a transconductance amplifier for detecting a difference between a sensed current and a command current. As such, Mortazavi's amplifier 66 is not a current sense amplifier that is coupled to the transconductance amplifier that detects an error current from a sensed current and a command current. This is because amplifier 56 in Mortazavi does not detect an error current by comparing a sensed current and a command current. Therefore, for at least the above additional reasons, Applicant believes that Claim 3 is patentably distinguishable from Baker, Vitunic and Mortazavi (alone and in combination).

With respect to Claim 6, Vitunic (Fig. 7: Capacitor 250) does not disclose that the "compensator includes a capacitor," as required by Claim 6, because the capacitor 250 is not a compensator as claimed. Neither does Mortazavi (Fig. 2: 56 and C4) disclose such limitations because any compensator in Mortazavi does not integrate an error current into a coil current, as claimed. Accordingly, for at least the above reasons, Applicant submits that Claim 6 is patentably distinguishable from Baker, Vitunic and Mortazavi (alone and in combination).

With respect to Claim 11, as noted above, Vitunic (Fig. 7: Capacitor 250) does not disclose that a compensator is coupled to a transconductance amplifier that detects an error current from a sensed coil current and a command current, and that the compensator includes a capacitor, as required by Claim 11. The capacitor 250 in Vitunic is not a compensator and the amplifier 234 is not a transconductance amplifier. Mortazavi (Fig. 2: 56, C4, 64) does disclose the missing limitations because the compensator in Mortazavi does not integrate an error current into a coil current. Further, the driver amplifier 64 is not a transconductance amplifier that detects an error current from a sensed coil current and a command current. Therefore, for at least these additional reasons, Applicant believes that Claim 11 is patentably distinguishable from Baker, Vitunic and Mortazavi (alone and in combination).

With respect to Claim 13, the references do not disclose that the "compensator is coupled to a gain buffer," as required by Claim 13. The buffer 46 in Fig. 1 of Mortazavi is simply a cache memory buffer chip for data storage during data transfer between a data disk in a disk drive and a host computer (Col. 6, lines 1-4). The memory chip 46 is not a gain buffer and has nothing to do with a gain buffer relating to loop gain. Furthermore, there is no indication in Mortazavi that any compensator is coupled to the memory chip 46. In addition, the Examiner has not explained where in Mortazavi the memory chip 46 is used transfer data such as gain data. Also, in Col. 7, lines 13-25 of Mortazavi, there is no mention of a gain buffer whatsoever. The Examiner has not explained why gain information relating to motor driver amplifiers are transferred to a host computer via memory chip 46. The Examiner has not explained how adding a memory chip 46 for user data transfer between a data disk and host computer to Baker and Vitunic, would in any way improve control of velocity, acceleration and deceleration.

Therefore, for at least these reasons, Applicant submits that Claim 13 is patentably distinguishable from Baker, Vitunic and Mortazavi (alone and in combination).

V. Rejection of Claims 14-18 and 20-22 Under 35 U.S.C. § 103(a)

Claims 14-18 and 20-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mortazavi in view of Baker and Vitunic. Applicant respectfully traverses the Examiner's rejection.

With respect to Claim 14, Mortazavi does not disclose determining an error current by comparing a coil current and a command current, as claimed therein. Also, Mortazavi does not disclose integrating an error current into a coil current. Further, as discussed above with regard to Claim 1, Baker does not disclose sensing a coil current and determining an error current by comparing said coil current and a command current. And, as noted above, Vitunic does not disclose integrating an error current into a coil current, wherein the error current is determined by comparing a sensed coil current and a command current.

For at least the above reasons, Applicant submits that Claim 14 is patentably distinguishable from Mortazavi, Baker and Vitunic (alone and in combination). For at least the same reasons, Applicant believes that the claims that depend from Claim 14 (i.e., Claims 15-18 and 20-22) are likewise patentably distinguishable from Mortazavi, Baker and Vitunic (alone and in combination). Nevertheless, some of the claims that depend from Claim 14 may also be allowable for additional reasons and some of those reasons are provided below.

With respect to Claim 16, Applicant submits that Mortazavi fails to disclose "receiving said command current at said driver," as required by Claim 16. The Examiner cites Col. 4, lines 47-48 of Mortazavi as disclosing the required limitation. However, Col. 4, lines 47-48 of

Mortazavi simply mentions "applying the compensated control value to control the H-bridge driver during linear mode operations." This has nothing to do with the claimed limitation of "receiving said command current at said driver," as required by Claim 16. For at least this additional reason, Applicant submits that Claim 16 is patentably distinguishable from Mortazavi, Baker and Vitunic (alone and in combination).

With respect to Claim 18, Applicant submits that Mortazavi does not disclose "sensing a voltage and determining said coil current from said voltage," as required by Claim 18. The Examiner stated that the limitation was disclosed in Col. 7, lines 35-47 of Mortazavi. However, Col. 7, lines 35-47 of Mortazavi clearly indicates that the output of the amplifier 66 (Fig. 2) is a voltage in relation to vref at the input of the amplifier 56. There is no mention whatsoever of "sensing a voltage and determining said coil current from said voltage," as required by Claim 18. For at least this additional reason, Applicant submits that Claim 18 is patentably distinguishable from Mortazavi, Baker and Vitunic (alone and in combination).

VI. Rejection of Claims 23-29 under 35 U.S.C. § 103(a)

The Examiner rejected Claims 23-29 under 35 U.S.C. § 103(a) as being unpatentable over Mortazavi in view of Baker. Applicant respectfully traverses the rejection.

With respect to Claim 23, as discussed above, Baker does not disclose detecting an error current by comparing a command current and a coil current, as required by Claim 23 (as amended). Further, as noted above, Mortazavi does not disclose a compensator that integrates such an error current with a command current. Even further, Applicant believes that Mortazavi cannot be modified by Baker because Mortazavi is directed to PWM/linear driver for a disk drive voice coil actuator. This is not in any way related to Baker's circuit in which FET sense currents

are used to provide adaptive, closed-loop clamping of the drive voltages at levels sufficient to maintain the non-load current conducting transistors in a quiescent state. For at least the above reasons, Applicant submits that Claim 23 is patentably distinguishable from Mortazavi and Baker, both alone and in combination. For at least the same reasons, Applicant submits that the claims that depend from Claim 23 (i.e., Claims 24-28) are likewise patentably distinguishable from Mortazavi and Baker, both alone and in combination. Furthermore, some of the dependent claims may also be allowable for additional reasons and some of those reasons are provided below.

With respect to Claim 24, as discussed above, Baker does not disclose "a transconductance amplifier to detect and calculate said error current by comparing said command current and said coil current," as required by Claim 24 (as amended). For at least these reasons, Claim 24 is patentably distinguishable from Mortazavi and Baker, both alone and in combination.

VII. Rejection of Claim 29 Under 35 U.S.C. § 103(a)

Claim 29 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Mortazavi in view of Vitunic. Applicant traverses the rejection.

Applicant submits that Mortazavi does not disclose "a transconductance amplifier coupled to said current sense amplifier to receive said voltage and a command current, wherein said transconductance amplifier calculates an error current by comparing the sense current with the command current," as required by Claim 29. Specifically, the compensation amplifier 56 in Fig. 2 of Mortazavi is not a transconductance amplifier that detects an error current by comparing a sensed coil current and a command current. Mortazavi describes that the amplifier

56 is a compensation amplifier that forms an integrator in conjunction with a capacitor C4 and a resistor R3 (Col. 6, lines 50-54).

Further, as described by Mortazavi and shown in Fig. 2, the sense current from amplifier 66 and the command current from the decoder & filter 54 are connected to only one input of the compensation amplifier 56 (Col. 6, lines 42-50 and Col. 7, lines 47-50). Therefore, by definition, the compensation amplifier 56 cannot calculate an error current by comparing said sensed coil current and the command current, as required by Claim 29. Further, the compensation amplifier 56 does not generate an error current. In addition, Mortazavi does not disclose that such a compensator 56 integrates said error current into said command current to determine said coil current.

Furthermore, as mentioned above, Vitunic does not teach "an integrator coupled to said transconductance amplifier to integrate said error current," which error current is calculated "by comparing said sense current and said command current," as required by Claim 29. For at least the above reasons, Applicant submits that Claim 29 is patentably distinguishable from Mortazavi and Vitunic, both alone and in combination.

VIII. Rejection of Claims 50, 55-58, 61 and 63 Under 35 U.S.C. § 103(a)

Claims 50, 57, 58, 61 and 63 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,422,027 to Mohlere (hereinafter "Mohlere") in view of U.S. Patent No. 5,821,717 to Hassan et al. (hereinafter "Hassan"). Applicant respectfully traverses the rejection.

With respect to Claim 50, Mohlere does not disclose "a driver for controlling a voice coil motor ... having a first coil motor and second coil motor," as required by Claim 50. It is

respectfully submitted that in Fig. 2 of Mohlere, items Unit 1 and Unit 2 are two different, independent, voice coil motors. Indeed, Mohlere states that: "[t]he controller can handle two motors as is shown in FIG. 2. Each of the two shown control computer (CPU) channels 101 and 100 controls 1 channel ... The Motor(s) get driven by the AMDRIVE signal hh. The Graticule Position Sensor 201 of unit 1 attached to the motor 202 sends back indicating signals ee, ff and gg from which the controller 203 computes position, direction, and velocity information. Unit 2 acts in the same manner as unit 1" (Col. 2, lines 34-44). Accordingly, Mohlere discloses two different, independent, voice coil motors that can be controlled, one at a time, by a controller.

Further, Hassan does not disclose "an error amplifier to calculate a differential between said velocity voltage and a command voltage," as required by Claim 50. Indeed, Hassan states that "[a] current control device 10, which may be, for example, a part of digital signal processing block 70, supplies an input voltage representative of the desired actuator current. This voltage is filtered by low pass filter 111. Sense amplifier 114 produces an output signal proportional to the actual current passing through actuator 300 by sensing and amplifying the voltage drop across sense resistor 310." (Col. 3, lines 12-19). Then, Hassan states that the "[e]rror amplifier 112 takes the difference between the output of sense amplifier 114 and the output of low pass filter 111" (Col. 3, lines 23-25). Accordingly, there is no velocity voltage sensing in Hassan, and Applicant submits that there is no use for it by modifying Hassan.

Further, Hassan does not disclose "a retract amplifier to compensate said command voltage with said differential," as required by Claim 50. In rejecting Claim 50, the Examiner relies on Item 113 in Fig. 2 of Hassan. Applicant submits, however, that there is no teaching in Hassan that Item 113 compensates a command voltage with a differential between the velocity voltage and the command voltage.

The Examiner further relies on Col. 5, lines 37-67 of Hassan in rejecting Claim 50. However, there is no description therein of a retract amplifier as required by Claim 50. In contrast, in that passage, Hassan states that:

> ... When the supply voltage drops below a threshold level, voltage monitor 133 sends a fault signal to actuator retract block 131.... [W]hen actuator retract block 131 receives a fault signal from voltage monitor 133 on input port 131a indicating a loss of supply voltage, an output signal is sent to actuator motor predrive amplifier 113 causing fast retraction of the read head. When a head retract is requested for some non-critical reason, a slower retraction is desirable so as to avoid potential damage to the read heads caused by sudden acceleration. Thus, when a retract signal is received on input port 131b, actuator retract block 131 sends an output signal to actuator motor predrive amplifier 113 causing slow retraction of the read head.

As such, Hassan does not use velocity for VCM coil current control. Further, Hassan's error amplifier 113 does not use a velocity voltage. Even further, the VCM retract amplifier 131 in Hassan is not a retract amplifier, as required by Claim 50.

In addition, there is no suggestion or motivation in either Mohlere or Hassan to combine such references. Even if Mohlere is combined with Hassan, the resulting combination does not disclose the claimed invention. This is because such a combination, if operational, may provide control for two different VCMs, and does not compensate a command voltage by a differential between a sensed velocity voltage and a command voltage. Accordingly, for at least the above reasons, Applicant submits that Claim 50 is patentably distinguishable from Mohlere and Hassan, both individually and in combination. For at least the same reasons, Applicant submits that the claims that depend from Claim 50 (i.e., Claims 51-57) are likewise patentably distinguishable from Mohlere and Hassan, both individually and in combination.

Claim 58 was rejected for substantially the same reasons as Claim 50. For reasons similar to those provided with respect to Claim 50, Applicant submits that Claim 50 is patentably distinguishable from Mohlere and Hassan. Similarly, Claims 59-63, which depend from Claim

58, are patentably distinguishable from Mohlere and Hassan for at least the same reasons as Claim 50.

Claims 55 and 56 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mohlere in view of Hassan as applied to Claim 50, and further in view of Mortazavi. Applicant submits that Claims 55 and 56 are patentably distinguishable from the aforementioned references at least because they depend from Claim 50.

IX. Information Disclosure Statement

Applicant mailed an Information Disclosure Statement, along with a completed Form PTO-1449 to the U.S. Patent Office on April 24, 2003. Applicant notes that Applicant has not yet received an initialed copy of the Form PTO-1449. Applicant requests the Examiner to forward a copy of same.

If the Examiner did not receive the Information Disclosure Statement, the Examiner is requested to contact the undersigned, who would be pleased to provide another copy of the Information Disclosure Statement (and accompanying materials) to the Examiner.

X. Additional Claim Fees

In determining whether additional claim fees are due, reference is made to the Fee Calculation Table (below).

Fee Calculation Table

	Claims Remaining After Amendment		Highest Number Previously Paid For	Present Extra	Rate	Additional Fee
Total (37 CFR 1.16(c))	100	Minus	100	= 0	x $18 =	$ 0.00
Independent (37 CFR 1.16(b))	16	Minus	16	= 0	x $86 =	$ 0.00

As set forth in the Fee Calculation Table (above), Applicant previously paid claim fees for one hundred (100) total claims and for sixteen (16) independent claims. Accordingly, Applicant believes that no additional fees are due. Nevertheless, Applicant hereby authorizes the Commissioner to charge Deposit Account No. 50-2198 for any fee deficiencies associated with filing this paper.

XI. Conclusion

Applicant believes that the application appears to be in form for allowance. Accordingly, reconsideration and allowance thereof is respectfully requested.

The Examiner is invited to contact the undersigned at the below-listed telephone number regarding any matters relating to the present application.

Respectfully submitted,

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